Appl. No. 10/761,985
Examiner: Tran, Thien F, Art Unit 2811
In response to the Office Action dated May 19, 2005

Date: August 16, 2005
Attorney Docket No. 10113681

AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 3, line 1 with the following amended paragraph:

– According to the object of the invention, a dynamic random access memory cell layout has a first ~~gate~~ conductor line pair and a second ~~gate~~ conductor line pair extending along a first direction, in which each conductor line pair comprises a first conductive line and a second conductive line, and in which each ~~gate conductor pair~~ conductive line comprises a ~~first~~ gate conductive line portion and a ~~second gate conductive~~ word line portion. A bitline pair has a first bitline and a second bitline, which extend along a second direction and intersect the ~~gate~~ conductor line pairs. Corresponding to the first bitline, a first active area extends along the second direction to cross the first ~~gate~~ conductor line pair. Corresponding to the second bitline, a second active area extends along the second direction to cross the second ~~gate~~ conductor line pair. Each active area has a first deep trench and a second deep trench formed in a substrate underneath the first ~~gate~~ conductive line and the second ~~gate~~ conductive line, respectively. A bitline contact is formed between the first ~~gate~~ conductive line and the second ~~gate~~ conductive line to be electrically connected to the corresponding bitline. A common source/drain region is formed in the substrate between the first ~~gate~~ conductive line and the second ~~gate~~ conductive line to be electrically connected to the bitline contact. A first vertical transistor and a second vertical transistor are formed overlying the first deep trench and the second deep trench, respectively. Each vertical transistor has a buried strap out-diffusion region formed in the substrate adjacent to one sidewall of the deep trench.